WHAT IS CLAIMED IS:

1. An arrangement for retaining data output from a main circuit throughout a low power mode and for restoring the retained data to the main circuit upon termination of the low power mode, the arrangement comprising:

a slave latch configured to store the data output from the main circuit as the retained data throughout the low power mode; and

a control portion configured to restore the retained data to the main circuit through Set and Reset inputs to the main circuit, so as to unambiguously determine restored data output upon the termination of the low power mode.

2. The arrangement of Claim 1, wherein:

the main circuit is a main latch that receives at its Set and Reset inputs, Set and Reset signals that have values matching those of the retained data; and

the Set and Reset signals directly control at least one main latch data output without delay other than a logic gate propagation delay.

3. The arrangement of Claim 2, wherein:

the Set and Reset signals are stably asserted before power is stably restored to the main latch.

4. The arrangement of Claim 2, wherein:

the Set and Reset signals are of opposite value, so as to prevent data contention in the main latch when the retained data is restored to the main latch.

5. The arrangement of Claim 4, wherein:

the Set and Reset signals have values that are the same as the retained data.

6. The arrangement of Claim 2, wherein the control portion includes:

first and second switches whose respective control inputs are controlled by a Restore signal that is active only during an activation delay period following the low power mode; and

third and fourth switches whose respective control inputs are controlled by the retained data;

wherein the first and third switches are connected between a first constant voltage level and a first one of the Set and Reset signals; and

wherein the second and fourth switches are connected between the first constant voltage level and a second one of the Set and Reset signals.

7. The arrangement of Claim 6, wherein:

the first, second, third and fourth switches are n-channel MOSFETs.

8. The arrangement of Claim 6, further comprising:

fifth and sixth switches that are connected between a second constant voltage level and the first one of the Set and Reset signals, and whose respective control inputs are controlled by the Restore signal and the second one of the Set and Reset signals; and

seventh and eighth switches that are connected between the second constant voltage level and the second one of the Set and Reset signals, and whose respective control inputs are controlled by the Restore signal and the first one of the Set and Reset signals.

9. The arrangement of Claim 8, wherein:

the fifth, sixth, seventh and eighth switches are p-channel MOSFETs.

10. The arrangement of Claim 2, further comprising:

a) ninth and tenth switches that are connected between a first input of the slave latch and a first constant voltage level, and whose respective control inputs are controlled by:

1) a Save signal that is active only during a normal mode that is distinct from the low power mode; and

2) a first of the main circuit's data outputs; and

b) eleventh and twelfth switches that are connected between a second input of the slave latch and the first constant voltage, and whose respective control inputs are controlled by the Save signal and a second of the main circuit's data outputs.

11. The arrangement of Claim 10, wherein:

the ninth, tenth, eleventh and twelfth switches are n-channel MOSFETs.

12. The arrangement of Claim 2, wherein:

the slave latch requires for its operation only a single input for each data output of the main circuit, so as to minimize loading of the main circuit's data output(s).

13. The arrangement of Claim 2, wherein:

the slave latch includes transistors that are all from a group including low leakage transistors and long channel transistors, so as to minimize power consumption.

14. The arrangement of Claim 2, wherein:

the main circuit is a latch circuit including two cross-coupled logic gates that receive respective ones of the Set and Reset signals.

15. The arrangement of Claim 2, wherein:

in a normal mode distinct from the low power mode, the slave latch and main circuit store input data concurrently.

16. The arrangement of Claim 1, wherein:

the slave latch requires for its operation only a single input for each data output of the main circuit, so as to minimize loading of the main circuit's data output(s).

17. The arrangement of Claim 1, wherein:

the slave latch includes transistors that are all from a group including low leakage transistors and long channel transistors, so as to minimize power consumption.

18. The arrangement of Claim 1, wherein:

the main circuit is a latch circuit including two cross-coupled logic gates that each receive one of Set and Reset signals that completely control the data output upon the termination of the low power mode.

19. The arrangement of Claim 1, wherein:

in a normal mode distinct from the low power mode, the slave latch and main circuit store input data concurrently.

20. The arrangement of Claim 1, further comprising:

a Retain voltage source that continuously provides power to the slave latch, even during the low power mode.

21. A method for retaining data output from a main circuit throughout a low power mode and for restoring the retained data to the main circuit upon termination of the low power mode, the method comprising:

storing the data output from the main circuit into a slave latch as the retained data throughout the low power mode; and

restoring the retained data to the main circuit through Set and Reset inputs to the main circuit, so as to unambiguously determine restored data output upon the termination of the low power mode.

22. The method of Claim 21, wherein the restoring step includes:

receiving, at Set and Reset inputs of the main circuit, Set and Reset signals that have values matching those of the retained data; and

with the Set and Reset signals, directly controlling at least one main circuit data output without delay other than a logic gate propagation delay.

23. The method of Claim 22, further comprising:

stably asserting the Set and Reset signals before stably restoring power to the main circuit.

24. The method of Claim 22, further comprising:

in a normal mode distinct from the low power mode, concurrently storing input data into the slave latch and into the main circuit.